FIG.1

1000

142

200

230 WRITE DATA CONVERSION CIRCUIT

220 READ DATA CONVERSION CIRCUIT

210 CONTROL CIRCUIT

DQ0 10 DQj
14 144
A0 12 Ak

146

110 ROW DECODER

130 COLUMN DECODER

DATA LATCH R (DL-R)

MEMORY ARRAY PART

100R ROW DECODER

110

130

SENSE LATCH (SL)

COLUMN DECODER

18

120

130

COLUMN DECODER

110 ROW DECODER

WL BL

MEMORY ARRAY PART

BL WL

100L ROW DECODER

110

130 COLUMN DECODER

DATA LATCH L (DL-L)

20

POWER SUPPLY GENERATION PART

150

132

FIG.2

	IN-CELL DATA			I/O DATA		I/O DATA
MC0	"11"	1		0	1	0
MC1	"01"	0		1	0	1
MC2	"00"	0	→	2	0	2
MC3	"10"	1		3	1	3
MC4	"01"	0		4	0	4
MC5	"00"	0		5	0	5
MC6	"10"	1		6	1	6
MC7	"11"	1		7	1	7
		SL			DL-L	DL-R

OUTPUT
(C9h)

FIG.3

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

DATA "00" ⟩ LEVEL 3

- - - - - - - - - - - - - - - - - - DETERMINATION LEVEL Vj2

DATA "10" ⟩ LEVEL 2

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.4

DATA			I/O DATA		I/O DATA	
1		0	1	0	1	
0	→	1	0	1	0	
0		2	0	2	0	
0		3	1	3	0	
0		4	0	4	0	
0		5	0	5	0	
0		6	1	6	0	
1		7	1	7	1	
SL			DL-L		DL-R	

OUTPUT
(C9h)

FIG.5

THRESHOLD (V)

DATA "01" ⟹ LEVEL 4

DATA "00" ⟹ LEVEL 3

DATA "10" ⟹ LEVEL 2

------------------------------- DETERMINATION 1

DATA "11" ⟹ LEVEL 1

BIT NUMBER

FIG.6

```
DATA                    I/O DATA    I/O DATA
┌───┐                   0  ┌───┐    0  ┌───┐
│ 1 │                      │ 1 │       │ 1 │
├───┤      ─────────>   1  ├───┤    1  ├───┤
│ 0 │                      │ 0 │       │ 1 │
├───┤    OPERATION     2  ├───┤    2  ├───┤
│ 1 │                      │ 0 │       │ 0 │
├───┤                   3  ├───┤    3  ├───┤
│ 1 │                      │ 1 │       │ 0 │
├───┤                   4  ├───┤    4  ├───┤
│ 0 │                      │ 0 │       │ 1 │
├───┤                   5  ├───┤    5  ├───┤
│ 1 │                      │ 0 │       │ 0 │
├───┤                   6  ├───┤    6  ├───┤
│ 1 │                      │ 1 │       │ 0 │
├───┤                   7  ├───┤    7  ├───┤
│ 1 │                      │ 1 │       │ 1 │
└───┘                      └───┘       └───┘
 SL                       DL-L        DL-R
                         OUTPUT
                          (C9h)
```

FIG.7


```
THRESHOLD (V)    DATA "01"  ──>  LEVEL 4
                 - - - - - - - - - - - - - - DETERMINATION 3
                 DATA "00"  ──>  LEVEL 3
                 DATA "10"  ──>  LEVEL 2
                 DATA "11"  ──>  LEVEL 1
                 BIT NUMBER
```

OUTPUT (93h)
AFTER DATA OUTPUT
FROM DL-L

FIG.8

FIG.8

Timing chart showing:

SENSE LATCH SL: READ·STORE AT LEVEL 2 | CLEAR | READ·STORE AT LEVEL 1 | CLEAR | READ·STORE AT LEVEL 3

DATA LATCH DL-L

READ DATA CONVERSION CIRCUIT: OPERATION

DATA LATCH DL-R: STORE, STORE, RESULT

DATA OUTPUT (DQ0-7): DATA OUTPUT (1/2 SECTOR: FRONT HALF), DATA OUTPUT (1/2 SECTOR: REAR HALF)

Time markers: t1, t2, t3, t4, t5, t6, t7, t8, t9, t10

FIG.9

THRESHOLD (V)

DATA "10" ⊃ LEVEL 4

DATA "01" ⊃ LEVEL 3

DATA "11" ⊃ LEVEL 2

DATA "00" ⊃ LEVEL 1

BIT NUMBER

FIG.10

THRESHOLD (V)

DATA "10" ⊃ LEVEL 4

DATA "01" ⊃ LEVEL 3

DATA "00" ⊃ LEVEL 2

DATA "11" ⊃ LEVEL 1

BIT NUMBER

FIG.11

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

DATA "10" ⟩ LEVEL 3

DATA "00" ⟩ LEVEL 2

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.12

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

DATA "10" ⟩ LEVEL 3

DATA "11" ⟩ LEVEL 2

DATA "00" ⟩ LEVEL 1

BIT NUMBER

FIG.13

IN-CELL DATA

				I/O DATA			I/O DATA	
"11"	1		0	1		0	1	
"00"	0	"0" ONLY	1	0		1	1	
"01"	0	WHEN "0"	2	0		2	1	
"10"	0	IN SL AND	3	1		3	0	
"00"	0	"1" IN DL-R	4	0		4	1	
"01"	0		5	0		5	1	
"10"	0		6	1		6	0	
"11"	1		7	1		7	1	

SL

DL-L
OUTPUT
(C9h)

DL-R

FIG.14

THRESHOLD (V)

DATA "00" ⟩ LEVEL 4

DATA "01" ⟩ LEVEL 3

DATA "10" ⟩ LEVEL 2

- DETERMINATION 1

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.15

FIG.16A

120

SL

WL

BL1
BL2

FIG.16B

120

SL

WL

BL1
BL2

FIG.17

SLm   SLm+1

120

TGm   TGm+1   STG

MBLm   MBLm+1

Tr1m   Tr1m+1

BSS1

BSS2   Tr2m   Tr2m+1

MC1nm   MC2nm   MC1nm+1   MC2nm+1

WLn

WLn+1

WLn+2

64 cell

SBL1m   SBL2m   SBL1m+1   SBL2m+1

FIG.18

	DATA			I/O DATA		I/O DATA
MC1$_{n0}$	1		0	1	0	
MC1$_{n1}$	0	→	1	0	1	
MC1$_{n2}$	0		2	0	2	
MC1$_{n3}$	1		3	1	3	
MC1$_{n4}$	0		4	0	4	
MC1$_{n5}$	0		5	0	5	
MC1$_{n6}$	1		6	1	6	
MC1$_{n7}$	1		7	1	7	
	SL			DL-L		DL-R

OUTPUT
(C9h)

FIG.19

DATA "01" → LEVEL 4

DATA "00" → LEVEL 3

THRESHOLD (V) ---------------------------------- DETERMINATION 2

DATA "10" → LEVEL 2

DATA "11" → LEVEL 1

BIT NUMBER

FIG.20

```
DATA                I/O DATA    I/O DATA
┌───┐              0 ┌───┐    0 ┌───┐
│ 1 │                │ 1 │      │ 1 │
├───┤              1 ├───┤    1 ├───┤
│ 0 │                │ 0 │      │ 0 │
├───┤              2 ├───┤    2 ├───┤
│ 0 │     ──→        │ 0 │      │ 0 │
├───┤              3 ├───┤    3 ├───┤
│ 1 │                │ 1 │      │ 1 │
├───┤              4 ├───┤    4 ├───┤
│ 0 │                │ 0 │      │ 0 │
├───┤              5 ├───┤    5 ├───┤
│ 0 │                │ 0 │      │ 0 │
├───┤              6 ├───┤    6 ├───┤
│ 1 │                │ 1 │      │ 1 │
├───┤              7 ├───┤    7 ├───┤
│ 1 │                │ 1 │      │ 1 │
└───┘                └───┘      └───┘
 SL                  DL-L       DL-R
                    OUTPUT
                    (C9h)
```

FIG.21

```
          ↑
          │    ┌─────────────┐
          │    │ DATA "01"   │──→  LEVEL 4
          │    └─────────────┘
          │    ┌─────────────┐
          │    │ DATA "00"   │──→  LEVEL 3
THRESHOLD (V) ├─ - - - - - - - - - - - - - - - DETERMINATION 2
          │    │ DATA "10"   │──→  LEVEL 2
          │    └─────────────┘
          │    ┌─────────────┐
          │    │ DATA "11"   │──→  LEVEL 1
          │    └─────────────┘
          └──────────────────────→
              BIT NUMBER

          OUTPUT (C9h)
          AFTER DATA OUTPUT
          FROM DL-L
```

FIG.22

DATA		I/O DATA		I/O DATA	
1		0	1	0	1
0		1	0	1	0
0		2	0	2	0
0		3	0	3	1
0		4	0	4	0
0		5	0	5	0
0		6	0	6	1
1		7	1	7	1
SL		DL-L		DL-R	

OUTPUT
(C9h)

FIG.23

THRESHOLD (V)

DATA "01" ▷ LEVEL 4

DATA "00" ▷ LEVEL 3

DATA "10" ▷ LEVEL 2

---------------------------------- DETERMINATION 1

DATA "11" ▷ LEVEL 1

BIT NUMBER

FIG.24

DATA

| 1 |
| 0 |
| 1 |
| 1 |
| 0 |
| 1 |
| 1 |
| 1 |

SL

→ OPERATION →

I/O DATA

0	1
1	1
2	0
3	0
4	1
5	0
6	0
7	1

DL-L

OUTPUT
AFTER DATA
OUTPUT
FROM DL-R
(93h)

I/O DATA

0	1
1	0
2	0
3	1
4	0
5	0
6	1
7	1

DL-R

OUTPUT (C9h)

FIG.25

THRESHOLD (V)

DATA "01" ⇒ LEVEL 4

-------- DETERMINATION 3

DATA "00" ⇒ LEVEL 3

DATA "10" ⇒ LEVEL 2

DATA "11" ⇒ LEVEL 1

BIT NUMBER

FIG.26

DATA			I/O DATA		I/O DATA	
1		0	1	0	1	
0		1	1	1	0	
0		2	0	2	0	
0		3	0	3	0	
0		4	1	4	0	
0		5	0	5	0	
0		6	0	6	0	
1		7	1	7	1	

SL

DL-L

OUTPUT
(93h)

DL-R

FIG.27

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

DATA "00" ⟩ LEVEL 3

DATA "10" ⟩ LEVEL 2

- - - - - - - - - - - - - - - - - - - DETERMINATION 1

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.28

DATA

| 1 |
| 0 |
| 1 |
| 1 |
| 0 |
| 1 |
| 1 |
| 1 |

SL

→ OPERATION →

I/O DATA

0	1
1	1
2	0
3	0
4	1
5	0
6	0
7	1

DL-L
OUTPUT (93h)

I/O DATA

0	1
1	1
2	0
3	0
4	1
5	0
6	0
7	1

DL-R
OUTPUT (93h)
AFTER DATA
OUTPUT
FROM DL-L

FIG.29

THRESHOLD (V)

DATA "01" ⊳ LEVEL 4
------------------------ DETERMINATION 3
DATA "00" ⊳ LEVEL 3

DATA "10" ⊳ LEVEL 2

DATA "11" ⊳ LEVEL 1

BIT NUMBER

FIG.30

FIG.31

I/O DATA		I/O DATA		DATA	
0	1	0			1
1	0	1			0
2	0	2			0
3	1	3			1
4	0	4			0
5	0	5			0
6	1	6			1
7	1	7			1
	DL-L		DL-R		SL

INPUT (C9h)

FIG.32

THRESHOLD (V) — DATA "00" LEVEL 3 — DETERMINATION 2

DATA "11" LEVEL 1

BIT NUMBER

FIG.33

I/O DATA		I/O DATA			DATA	
0	1	0	1		1	
1	0	1	1		0	
2	0	2	0	OPERATION →	1	
3	1	3	0		1	
4	0	4	1		0	
5	0	5	0		1	
6	1	6	0		1	
7	1	7	1		1	

DL-L   DL-R   SL

INPUT (93h)

FIG.34

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

---------- DETERMINATION 3

DATA "00" ⟩ LEVEL 3

---------- DETERMINATION 2

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.35

I/O DATA		I/O DATA			DATA	
0	1	0	1		1	
1	0	1	1		1	
2	0	2	0	OPERATION →	1	
3	1	3	0		0	
4	0	4	1		1	
5	0	5	0		1	
6	1	6	0		0	
7	1	7	1		1	

DL-L   DL-R   SL

FIG.36

THRESHOLD (V)

DATA "01" → LEVEL 4

------------- DETERMINATION 3

DATA "00" → LEVEL 3

------------- DETERMINATION 2

DATA "10" → LEVEL 2

------------- DETERMINATION 1

DATA "11" → LEVEL 1

BIT NUMBER

FIG.37

DATA INPUT (DQ0-7)

DATA LATCH DL-L

WRITE DATA CONVERSION CIRCUIT

DATA LATCH DL-R

SENSE LATCH SL

DATA INPUT (1/2 SECTOR: FRONT HALF) | DATA INPUT (1/2 SECTOR: REAR HALF)

STORE

STORE

OPERATION 1

OPERATION 2

STORE | WRITE AT LEVEL 2 | CLEAR

STORE | WRITE AT LEVEL 3 | CLEAR | STORE | WRITE AT L

STORE | WRITE AT L

t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14

FIG.38

```
I/O DATA          DATA
  0 │ 1 │          │ 1 │
  1 │ 1 │          │ 0 │
  2 │ 0 │ ←OPERATION→ │ 0 │
  3 │ 0 │          │ 1 │
  4 │ 1 │          │ 0 │
  5 │ 0 │          │ 0 │
  6 │ 0 │          │ 1 │
  7 │ 1 │          │ 1 │
   DL-L             SL
INPUT (93h)     READ AT
               DETERMINATION 2
```

FIG.39

THRESHOLD (V)

DATA "00" ──▷ LEVEL 3

- - - - - - - - - - - - - - - - - - DETERMINATION 2

DATA "11" ──▷ LEVEL 1

BIT NUMBER

FIG.40

FIG.41

FIG.42

THRESHOLD (V)

DATA "011" ⊃ LEVEL 8
--------------------------------- DETERMINATION 7
DATA "010" ⊃ LEVEL 7
--------------------------------- DETERMINATION 6
DATA "000" ⊃ LEVEL 6
--------------------------------- DETERMINATION 5
DATA "001" ⊃ LEVEL 5
--------------------------------- DETERMINATION 4
DATA "101" ⊃ LEVEL 4
--------------------------------- DETERMINATION 3
DATA "100" ⊃ LEVEL 3
--------------------------------- DETERMINATION 2
DATA "110" ⊃ LEVEL 2
--------------------------------- DETERMINATION 1
DATA "111" ⊃ LEVEL 1

BIT NUMBER

MOST SIGNIFICANT BIT DEFINED
AT DETERMINATION 4
INTERMEDIATE BIT DEFINED
AT DETERMINATION 2 & 6
LEAST SIGNIFICANT BIT DEFINED
AT DETERMINATION 1, 3, 5 & 7

OK

FIG.43

THRESHOLD (V)

DATA "001" ⟩ LEVEL 8
------------------------------ DETERMINATION 7
DATA "000" ⟩ LEVEL 7
------------------------------ DETERMINATION 6
DATA "010" ⟩ LEVEL 6
------------------------------ DETERMINATION 5
DATA "011" ⟩ LEVEL 5
------------------------------ DETERMINATION 4
DATA "101" ⟩ LEVEL 4
------------------------------ DETERMINATION 3
DATA "100" ⟩ LEVEL 3
------------------------------ DETERMINATION 2
DATA "110" ⟩ LEVEL 2
------------------------------ DETERMINATION 1
DATA "111" ⟩ LEVEL 1

BIT NUMBER
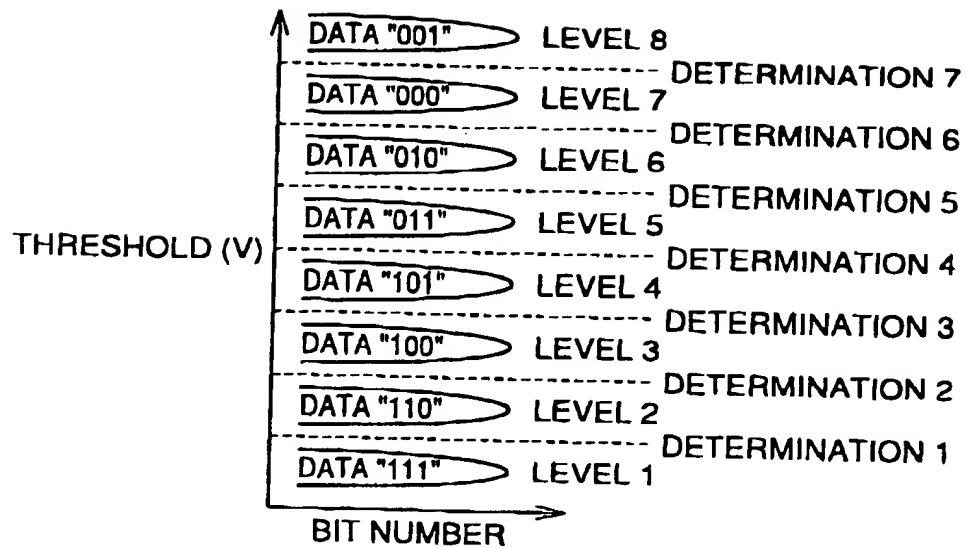
MOST SIGNIFICANT BIT DEFINED
AT DETERMINATION 4
"0" & "1" AT LEVELS 3, 4, 5 & 6
AT DETERMINATION 2 & 6
NOT DEFINED
LEAST SIGNIFICANT BIT DEFINED
AT DETERMINATION 1, 3, 5 & 7

NG

FIG.44

	IN-CELL DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA

MC0 "0111" [0]

MC1 "0110" [0]

MC2 "0100" [0]

MC3 "0101" [0]

MC4 "0001" [0]

MC5 "0000" [0]

MC6 "0010" [0]

MC7 "0011" [0]

MC8 "1011" [1]

MC9 "1010" [1]

MC10 "1000" [1]

MC11 "1001" [1]

MC12 "1101" [1]

MC13 "1100" [1]

MC14 "1110" [1]

MC15 "1111" [1]

SL

0 [0] 0
1 [0] 1
2 [0] 2
3 [0] 3
4 [0] 4
5 [0] 5
6 [0] 6
7 [0] 7
0 [1] 0
1 [1] 1
2 [1] 2
3 [1] 3
4 [1] 4
5 [1] 5
6 [1] 6
7 [1] 7

DL-1
OUTPUT
(00h-FFh)

0
1
2
3
4
5
6
7

DL-2

0
1
2
3
4
5
6
7

DL-3

0
1
2
3
4
5
6
7

DL-4

FIG.45

DATA "0111"	LEVEL 16
DATA "0110"	LEVEL 15
DATA "0100"	LEVEL 14
DATA "0101"	LEVEL 13
DATA "0001"	LEVEL 12
DATA "0000"	LEVEL 11
DATA "0010"	LEVEL 10
DATA "0011"	LEVEL 9
DATA "1011"	LEVEL 8
DATA "1010"	LEVEL 7
DATA "1000"	LEVEL 6
DATA "1001"	LEVEL 5
DATA "1101"	LEVEL 4
DATA "1100"	LEVEL 3
DATA "1110"	LEVEL 2
DATA "1111"	LEVEL 1

THRESHOLD (V)

DETERMINATION 8

BIT NUMBER

FIG.46

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA

```
DATA     I/O DATA   I/O DATA   I/O DATA   I/O DATA

 0          0  0      0  0      0          0
 0          1  0      1  0      1          1
 0   TO DL-2 2  0      2  0      2          2
 0          3  0      3  0      3          3
 0          4  0      4  0      4          4
 0          5  0      5  0      5          5
 0          6  0      6  0      6          6
 0          7  0      7  0      7          7
 0          0  1      0  0      0          0
 0          1  1      1  0      1          1
 0          2  1      2  0      2          2
 0          3  1      3  0      3          3
 1          4  1      4  1      4          4
 1          5  1      5  1      5          5
 1          6  1      6  1      6          6
 1          7  1      7  1      7          7

SL          DL-1      DL-2     DL-3       DL-4
            OUTPUT
            (00h-FFh)
```

FIG.47

THRESHOLD (V)

DATA "0111" ⇒ LEVEL 16

DATA "0110" ⇒ LEVEL 15

DATA "0100" ⇒ LEVEL 14

DATA "0101" ⇒ LEVEL 13

DATA "0001" ⇒ LEVEL 12

DATA "0000" ⇒ LEVEL 11

DATA "0010" ⇒ LEVEL 10

DATA "0011" ⇒ LEVEL 9

DATA "1011" ⇒ LEVEL 8

DATA "1010" ⇒ LEVEL 7

DATA "1000" ⇒ LEVEL 6

DATA "1001" ⇒ LEVEL 5

- DETERMINATION 4

DATA "1101" ⇒ LEVEL 4

DATA "1100" ⇒ LEVEL 3

DATA "1110" ⇒ LEVEL 2

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.48

DATA			I/O DATA		I/O DATA		I/O DATA	I/O DATA
0		0	0	0	0	0	0	0
0		1	0	1	0	1	1	1
0	NOR WITH	2	0	2	0	2	2	2
0	INVERTED	3	0	3	0	3	3	3
1	DATA OF SL	4	0	4	1	4	4	4
1	TO DL-2	5	0	5	1	5	5	5
1		6	0	6	1	6	6	6
1		7	0	7	1	7	7	7
1		0	1	0	1	0	0	0
1		1	1	1	1	1	1	1
1		2	1	2	1	2	2	2
1		3	1	3	1	3	3	3
1		4	1	4	0	4	4	4
1		5	1	5	0	5	5	5
1		6	1	6	0	6	6	6
1		7	1	7	0	7	7	7

SL

DL-1
OUTPUT
(00h-FFh)

DL-2
OUTPUT
AFTER
OUTPUT
FROM DL-1
(0Fh-F0h)

DL-3

DL-4

FIG.49

DATA "0111" ⟶ LEVEL 16

DATA "0110" ⟶ LEVEL 15

DATA "0100" ⟶ LEVEL 14

DATA "0101" ⟶ LEVEL 13

-- DETERMINATION 12

DATA "0001" ⟶ LEVEL 12

DATA "0000" ⟶ LEVEL 11

DATA "0010" ⟶ LEVEL 10

THRESHOLD (V) | DATA "0011" ⟶ LEVEL 9

DATA "1011" ⟶ LEVEL 8

DATA "1010" ⟶ LEVEL 7

DATA "1000" ⟶ LEVEL 6

DATA "1001" ⟶ LEVEL 5

DATA "1101" ⟶ LEVEL 4

DATA "1100" ⟶ LEVEL 3

DATA "1110" ⟶ LEVEL 2

DATA "1111" ⟶ LEVEL 1

BIT NUMBER

FIG.50

DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA
0		0	0	0	0	0	0	0
0		1	0	1	0	1	0	1
0	TO DL-3	2	0	2	0	2	0	2
0		3	0	3	0	3	0	3
0		4	0	4	1	4	0	4
0		5	0	5	1	5	0	5
0		6	0	6	1	6	0	6
0		7	0	7	1	7	0	7
0		0	1	0	1	0	0	0
0		1	1	1	1	1	0	1
0		2	1	2	1	2	0	2
0		3	1	3	1	3	0	3
0		4	1	4	0	4	0	4
0		5	1	5	0	5	0	5
1		6	1	6	0	6	1	6
1		7	1	7	0	7	1	7
SL		DL-1		DL-2		DL-3		DL-4

OUTPUT (00h-FFh)

OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)

FIG.51

THRESHOLD (V)

- DATA "0111" ⟩ LEVEL 16
- DATA "0110" ⟩ LEVEL 15
- DATA "0100" ⟩ LEVEL 14
- DATA "0101" ⟩ LEVEL 13
- DATA "0001" ⟩ LEVEL 12
- DATA "0000" ⟩ LEVEL 11
- DATA "0010" ⟩ LEVEL 10
- DATA "0011" ⟩ LEVEL 9
- DATA "1011" ⟩ LEVEL 8
- DATA "1010" ⟩ LEVEL 7
- DATA "1000" ⟩ LEVEL 6
- DATA "1001" ⟩ LEVEL 5
- DATA "1101" ⟩ LEVEL 4
- DATA "1100" ⟩ LEVEL 3
- DETERMINATION 2
- DATA "1110" ⟩ LEVEL 2
- DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.52

DATA		NOR WITH INVERTED DATA OF SL TO DL-3 →	I/O DATA	I/O DATA	I/O DATA	I/O DATA

```
DATA                          I/O DATA   I/O DATA   I/O DATA   I/O DATA
 0                          0   0      0   0      0   0      0
 0                          1   0      1   0      1   0      1
 0    NOR WITH              2   0      2   0      2   0      2
 0    INVERTED             3   0      3   0      3   0      3
 0    DATA OF SL           4   0      4   1      4   0      4
 0    TO DL-3              5   0      5   1      5   0      5
 0                          6   0      6   1      6   0      6
 0                          7   0      7   1      7   0      7
 0                          0   1      0   1      0   0      0
 0                          1   1      1   1      1   0      1
 1                          2   1      2   1      2   1      2
 1                          3   1      3   1      3   1      3
 1                          4   1      4   0      4   1      4
 1                          5   1      5   0      5   1      5
 1                          6   1      6   0      6   0      6
 1                          7   1      7   0      7   0      7

SL                        DL-1       DL-2       DL-3       DL-4
                          OUTPUT     OUTPUT
                          (00h-FFh)  AFTER
                                     OUTPUT
                                     FROM DL-1
                                     (0Fh-F0h)
```
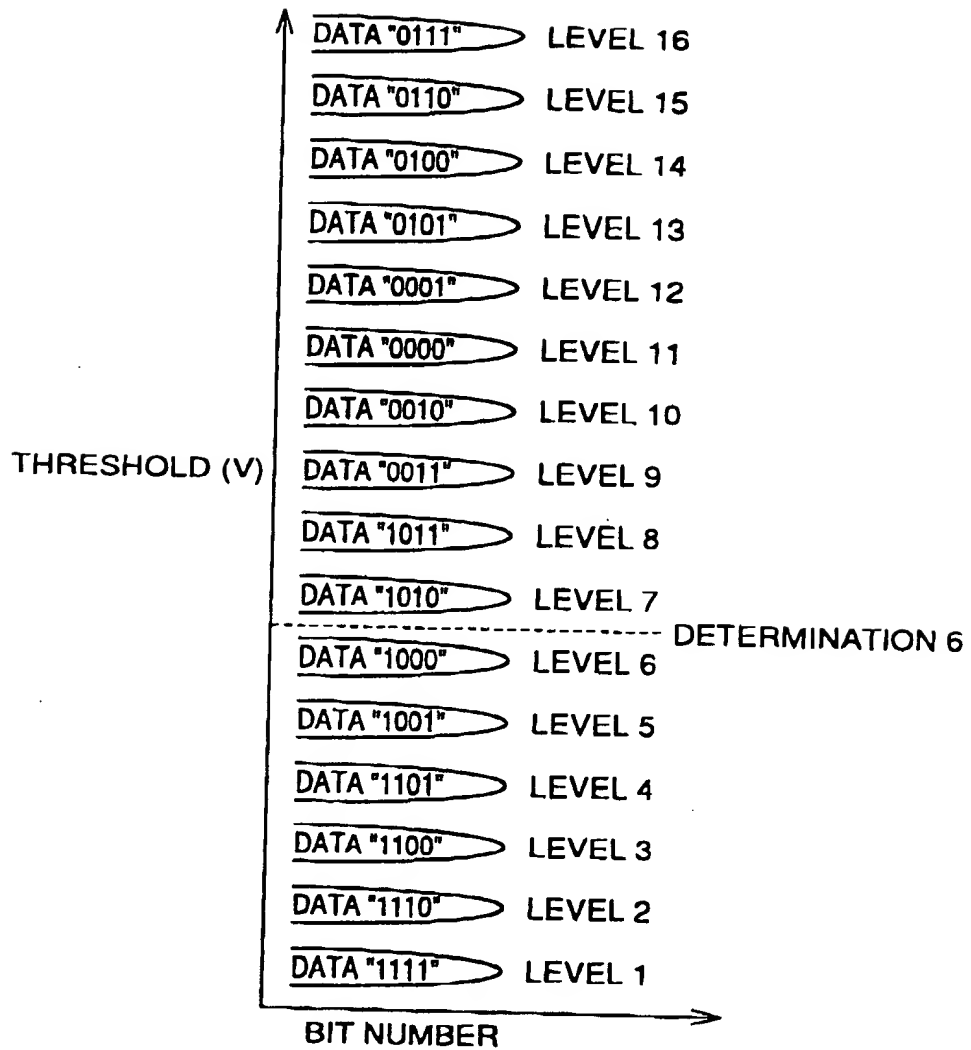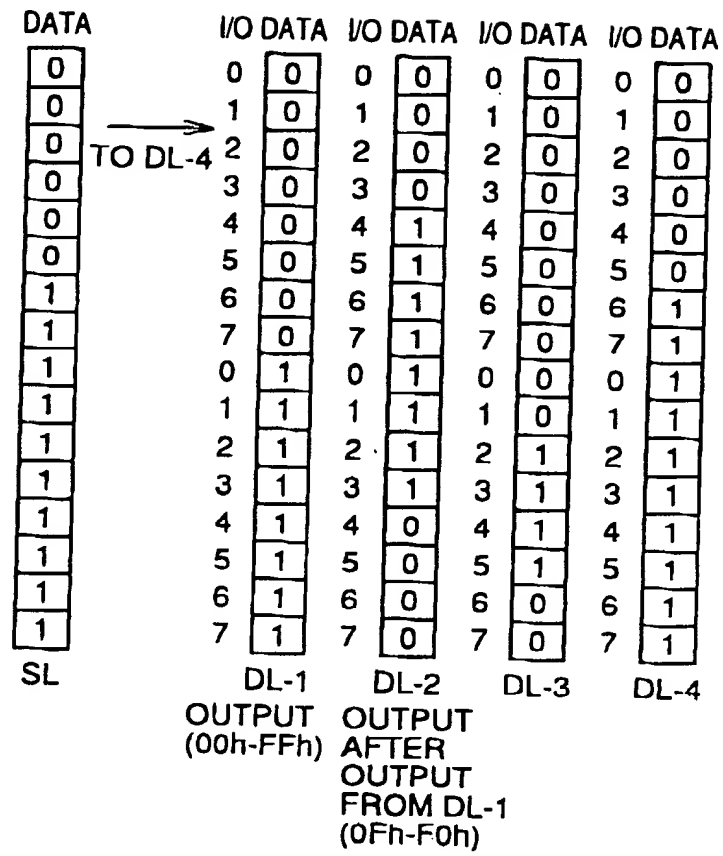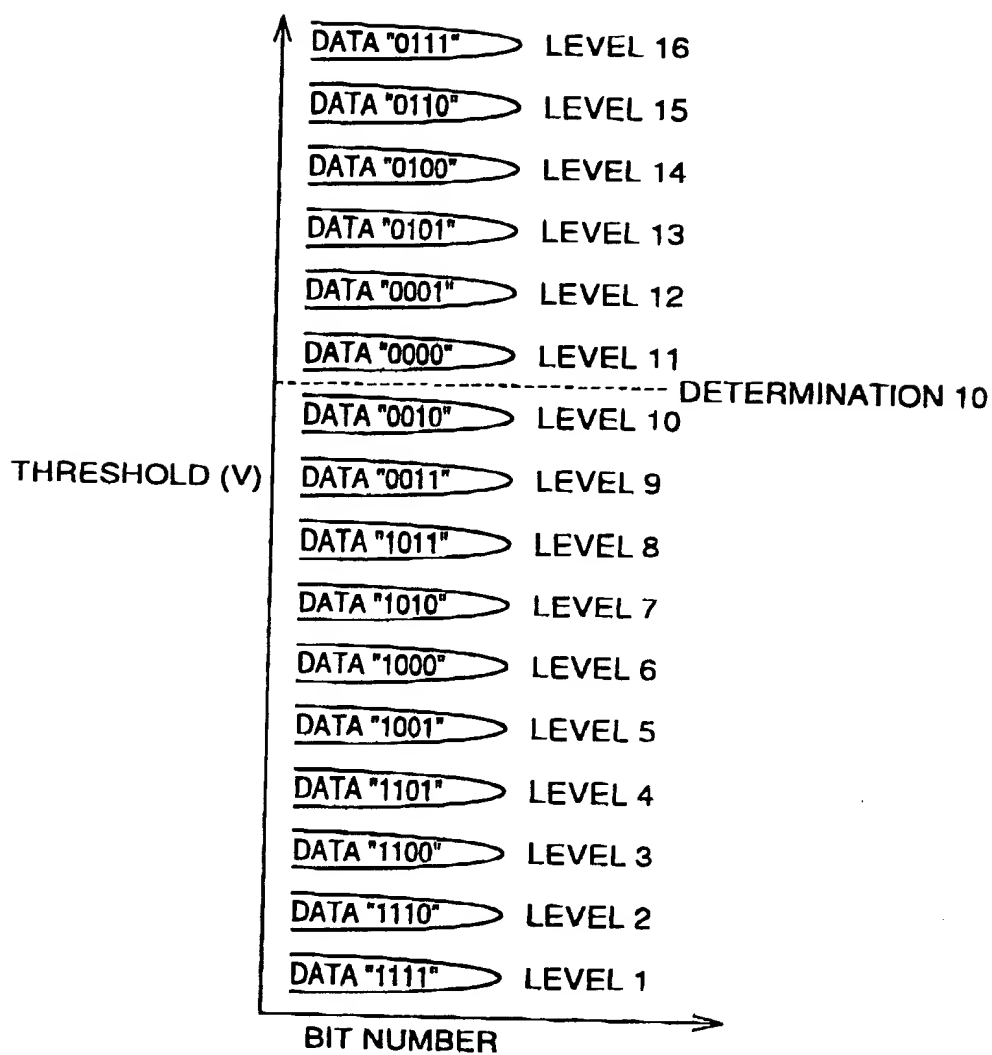
FIG.53

THRESHOLD (V)

DATA "0111" ⇒ LEVEL 16

DATA "0110" ⇒ LEVEL 15

DATA "0100" ⇒ LEVEL 14

DATA "0101" ⇒ LEVEL 13

DATA "0001" ⇒ LEVEL 12

DATA "0000" ⇒ LEVEL 11

DATA "0010" ⇒ LEVEL 10

DATA "0011" ⇒ LEVEL 9

DATA "1011" ⇒ LEVEL 8

DATA "1010" ⇒ LEVEL 7

- - - - - - - - - - - - - - - - - - - DETERMINATION 6

DATA "1000" ⇒ LEVEL 6

DATA "1001" ⇒ LEVEL 5

DATA "1101" ⇒ LEVEL 4

DATA "1100" ⇒ LEVEL 3

DATA "1110" ⇒ LEVEL 2

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.54

DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
0		0	0	0	0	0	0	0	0
0		1	0	1	0	1	0	1	0
0	TO DL-4	2	0	2	0	2	0	2	0
0		3	0	3	0	3	0	3	0
0		4	0	4	1	4	0	4	0
0		5	0	5	1	5	0	5	0
1		6	0	6	1	6	0	6	1
1		7	0	7	1	7	0	7	1
1		0	1	0	1	0	0	0	1
1		1	1	1	1	1	0	1	1
1		2	1	2	1	2	1	2	1
1		3	1	3	1	3	1	3	1
1		4	1	4	0	4	1	4	1
1		5	1	5	0	5	1	5	1
1		6	1	6	0	6	0	6	1
1		7	1	7	0	7	0	7	1
SL		DL-1		DL-2		DL-3		DL-4	

OUTPUT
(00h-FFh)

OUTPUT
AFTER
OUTPUT
FROM DL-1
(0Fh-F0h)

FIG.55

THRESHOLD (V)

DATA "0111" ▷ LEVEL 16

DATA "0110" ▷ LEVEL 15

DATA "0100" ▷ LEVEL 14

DATA "0101" ▷ LEVEL 13

DATA "0001" ▷ LEVEL 12

DATA "0000" ▷ LEVEL 11

------------------------------------- DETERMINATION 10

DATA "0010" ▷ LEVEL 10

DATA "0011" ▷ LEVEL 9

DATA "1011" ▷ LEVEL 8

DATA "1010" ▷ LEVEL 7

DATA "1000" ▷ LEVEL 6

DATA "1001" ▷ LEVEL 5

DATA "1101" ▷ LEVEL 4

DATA "1100" ▷ LEVEL 3

DATA "1110" ▷ LEVEL 2

DATA "1111" ▷ LEVEL 1

BIT NUMBER

FIG.56

DATA

		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
0		0	0	0	0	0	0	0	0
0		1	0 ·	1	0	1	0	1	0
1	NOR	2	0	2	0	2	0	2	1
1	INVERTED	3	0	3	0	3	0	3	1
1	DATA OF SL	4	0	4	1	4	0	4	1
1	AND DATA	5	0	5	1	5	0	5	1
1	OF DL-4	6	0	6	1	6	0	6	0
1	TO DL-4	7	0	7	1	7	0	7	0
1		0	1	0	1	0	0	0	0
1		1	1	1	1	1	0	1	0
1		2	1	2	1	2	1	2	0
1		3	1	3	1	3	0	3	0
1		4	1	4	0	4	1	4	0
1		5	1	5	0	5	1	5	0
1		6	1	6	0	6	0	6	0
1		7	1	7	0	7	0	7	0

SL   DL-1   DL-2   DL-3   DL-4

OUTPUT   OUTPUT
(00h-FFh) AFTER
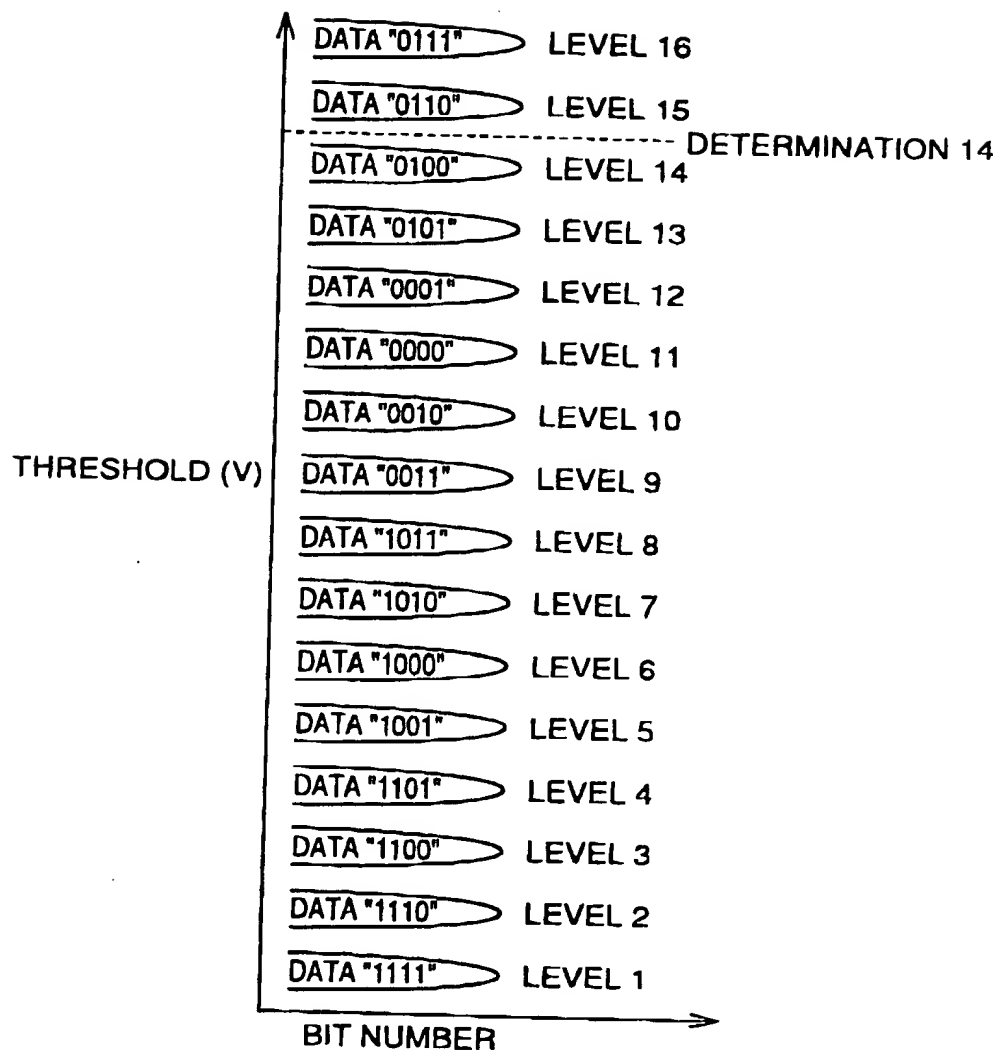   OUTPUT
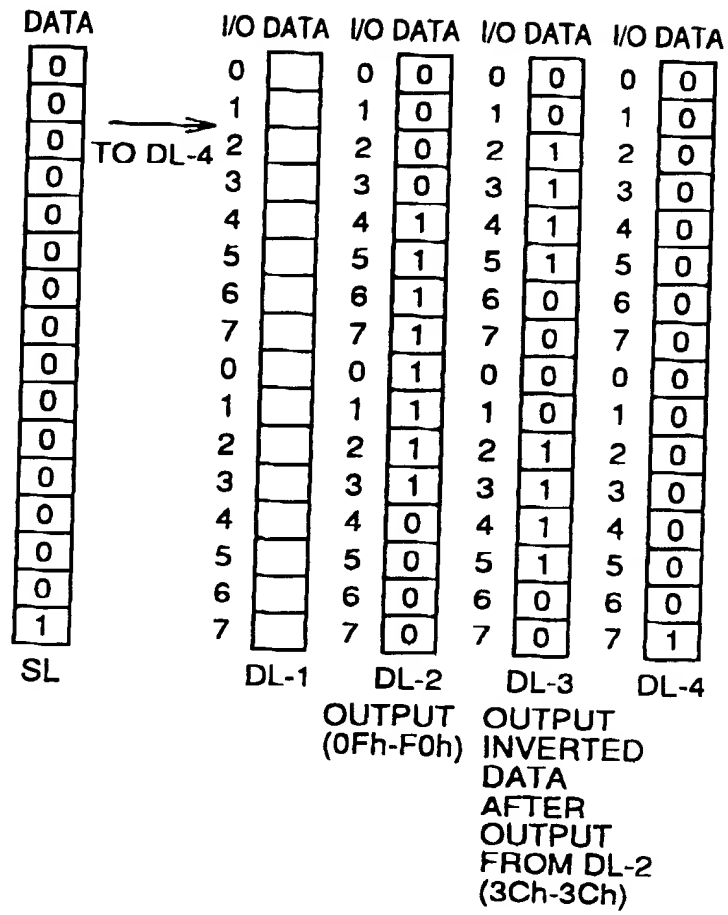   FROM DL-1
           (0Fh-F0h)

FIG.57

THRESHOLD (V)

DATA "0111" ⟩ LEVEL 16

DATA "0110" ⟩ LEVEL 15

- DETERMINATION 14

DATA "0100" ⟩ LEVEL 14

DATA "0101" ⟩ LEVEL 13

DATA "0001" ⟩ LEVEL 12

DATA "0000" ⟩ LEVEL 11

DATA "0010" ⟩ LEVEL 10

DATA "0011" ⟩ LEVEL 9

DATA "1011" ⟩ LEVEL 8

DATA "1010" ⟩ LEVEL 7

DATA "1000" ⟩ LEVEL 6

DATA "1001" ⟩ LEVEL 5

DATA "1101" ⟩ LEVEL 4

DATA "1100" ⟩ LEVEL 3

DATA "1110" ⟩ LEVEL 2

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.58

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
	0 [0]	0 [0]	0 [0]	0
	1 [0]	1 [0]	1 [0]	1
	2 [0]	2 [0]	2 [1]	2
	3 [0]	3 [0]	3 [1]	3
	4 [0]	4 [1]	4 [1]	4
	5 [0]	5 [1]	5 [1]	5
	6 [0]	6 [1]	6 [0]	6
	7 [0]	7 [1]	7 [0]	7
	0 [1]	0 [1]	0 [0]	0
	1 [1]	1 [1]	1 [0]	1
	2 [1]	2 [1]	2 [1]	2
	3 [1]	3 [1]	3 [1]	3
	4 [1]	4 [0]	4 [1]	4
	5 [1]	5 [0]	5 [1]	5
	6 [1]	6 [0]	6 [0]	6
	7 [1]	7 [0]	7 [0]	7
SL	DL-1	DL-2	DL-3	DL-4
	OUTPUT (00h-FFh)	OUTPUT AFTER OUTPUT FROM DL-1 (0Fh-F0h)	OR DATA OF DL-3 AND DL-4 AND STORE RESULT IN DL-3	

FIG.59

DATA "0111" ⇒ LEVEL 16

DATA "0110" ⇒ LEVEL 15

- DETERMINATION 14

DATA "0100" ⇒ LEVEL 14

DATA "0101" ⇒ LEVEL 13

DATA "0001" ⇒ LEVEL 12

DATA "0000" ⇒ LEVEL 11

DATA "0010" ⇒ LEVEL 10

THRESHOLD (V) | DATA "0011" ⇒ LEVEL 9

DATA "1011" ⇒ LEVEL 8

DATA "1010" ⇒ LEVEL 7

DATA "1000" ⇒ LEVEL 6

DATA "1001" ⇒ LEVEL 5

DATA "1101" ⇒ LEVEL 4

DATA "1100" ⇒ LEVEL 3

DATA "1110" ⇒ LEVEL 2

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.60

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0	0	0 0	0 0	0 0
0	1	1 0	1 0	1 0
0 → TO DL-4	2	2 0	2 1	2 0
0	3	3 0	3 1	3 0
0	4	4 1	4 1	4 0
0	5	5 1	5 1	5 0
0	6	6 1	6 0	6 0
0	7	7 1	7 0	7 0
0	0	0 1	0 0	0 0
0	1	1 1	1 0	1 0
0	2	2 1	2 1	2 0
0	3	3 1	3 1	3 0
0	4	4 0	4 1	4 0
0	5	5 0	5 1	5 0
0	6	6 0	6 0	6 0
1	7	7 0	7 0	7 1
SL	DL-1	DL-2	DL-3	DL-4

DL-2
OUTPUT
(0Fh-F0h)

DL-3
OUTPUT
INVERTED
DATA
AFTER
OUTPUT
FROM DL-2
(3Ch-3Ch)

FIG.61

THRESHOLD (V)

DATA "0111" ⟹ LEVEL 16

DATA "0110" ⟹ LEVEL 15

DATA "0100" ⟹ LEVEL 14

DATA "0101" ⟹ LEVEL 13

DATA "0001" ⟹ LEVEL 12

DATA "0000" ⟹ LEVEL 11

DATA "0010" ⟹ LEVEL 10

DATA "0011" ⟹ LEVEL 9

DATA "1011" ⟹ LEVEL 8

DATA "1010" ⟹ LEVEL 7

DATA "1000" ⟹ LEVEL 6

DATA "1001" ⟹ LEVEL 5

DATA "1101" ⟹ LEVEL 4

DATA "1100" ⟹ LEVEL 3

DATA "1110" ⟹ LEVEL 2

-------- DETERMINATION 1

DATA "1111" ⟹ LEVEL 1

BIT NUMBER

FIG.62

DATA

SL			I/O DATA DL-1	I/O DATA DL-2		I/O DATA DL-3		I/O DATA DL-4	
0		0		0	0	0	0	0	0
0		1		1	0	1	0	1	0
0	NOR	2		2	0	2	1	2	0
0	INVERTED	3		3	0	3	1	3	0
0	DATA OF SL	4		4	1	4	1	4	0
0	AND DATA	5		5	1	5	1	5	0
0	OF DL-4	6		6	1	6	0	6	0
0	TO DL-4	7		7	1	7	0	7	0
0		0		0	1	0	0	0	0
0		1		1	1	1	0	1	0
0		2		2	1	2	1	2	0
0		3		3	1	3	1	3	0
0		4		4	0	4	1	4	0
1		5		5	0	5	1	5	1
1		6		6	0	6	0	6	1
1		7		7	0	7	0	7	0

DL-2 OUTPUT (00h-FFh)

DL-3 OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)

FIG.63

THRESHOLD (V)

DATA "0111" ⇒ LEVEL 16
DATA "0110" ⇒ LEVEL 15
DATA "0100" ⇒ LEVEL 14
DATA "0101" ⇒ LEVEL 13
DATA "0001" ⇒ LEVEL 12
DATA "0000" ⇒ LEVEL 11
DATA "0010" ⇒ LEVEL 10
DATA "0011" ⇒ LEVEL 9
DATA "1011" ⇒ LEVEL 8
DATA "1010" ⇒ LEVEL 7
DATA "1000" ⇒ LEVEL 6
DATA "1001" ⇒ LEVEL 5
DATA "1101" ⇒ LEVEL 4
----------------------------------- DETERMINATION 3
DATA "1100" ⇒ LEVEL 3
DATA "1110" ⇒ LEVEL 2
DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.64

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
0				
0				
0	TO DL-1 →			
0				
0				
0				
0				
0				
0				
0				
0				
1				
1				
1				
1				
1				

I/O DATA columns:

DL-1: 0→0, 1→0, 2→0, 3→0, 4→0, 5→0, 6→0, 7→0, 0→0, 1→0, 2→0, 3→1, 4→1, 5→1, 6→1, 7→1

DL-2: 0→0, 1→0, 2→0, 3→0, 4→1, 5→1, 6→1, 7→1, 0→1, 1→1, 2→1, 3→1, 4→0, 5→0, 6→0, 7→0

DL-3: 0→0, 1→0, 2→1, 3→1, 4→1, 5→1, 6→0, 7→0, 0→0, 1→0, 2→1, 3→1, 4→1, 5→1, 6→0, 7→0

DL-4: 0→0, 1→0, 2→0, 3→0, 4→0, 5→0, 6→0, 7→0, 0→0, 1→0, 2→0, 3→0, 4→0, 5→1, 6→1, 7→0

SL

DL-1

DL-2
OUTPUT
(0Fh-F0h)

DL-3
OUTPUT
INVERTED
DATA
AFTER
OUTPUT
FROM DL-2
(3Ch-3Ch)

DL-4

FIG.65

THRESHOLD (V)

DATA "0111" ⟹ LEVEL 16

DATA "0110" ⟹ LEVEL 15

DATA "0100" ⟹ LEVEL 14

DATA "0101" ⟹ LEVEL 13

DATA "0001" ⟹ LEVEL 12

DATA "0000" ⟹ LEVEL 11

DATA "0010" ⟹ LEVEL 10

DATA "0011" ⟹ LEVEL 9

DATA "1011" ⟹ LEVEL 8

DATA "1010" ⟹ LEVEL 7

DATA "1000" ⟹ LEVEL 6

------------------------- DETERMINATION 5

DATA "1001" ⟹ LEVEL 5

DATA "1101" ⟹ LEVEL 4

DATA "1100" ⟹ LEVEL 3

DATA "1110" ⟹ LEVEL 2

DATA "1111" ⟹ LEVEL 1

BIT NUMBER

FIG.66

DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
0		0	0	0	0	0	0	0	0
0		1	0	1	0	1	0	1	0
0	NOR	2	0	2	0	2	1	2	0
0	INVERTED	3	0	3	0	3	1	3	0
0	DATA OF SL	4	0	4	1	4	1	4	0
0	AND DATA	5	0	5	1	5	1	5	0
0	OF DL-1	6	0	6	1	6	0	6	0
0	TO DL-1	7	0	7	1	7	0	7	0
0		0	0	0	1	0	0	0	0
1		1	1	1	1	1	0	1	0
1		2	1	2	1	2	1	2	0
1		3	0	3	1	3	1	3	0
1		4	0	4	0	4	1	4	0
1		5	0	5	0	5	1	5	1
1		6	0	6	0	6	0	6	1
1		7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	

OUTPUT
(00h-FFh)

OUTPUT
INVERTED
DATA
AFTER
OUTPUT
FROM DL-2
(00h-FFh)

FIG.67

THRESHOLD (V)

DATA "0111" ⊳ LEVEL 16

DATA "0110" ⊳ LEVEL 15

DATA "0100" ⊳ LEVEL 14

DATA "0101" ⊳ LEVEL 13

DATA "0001" ⊳ LEVEL 12

DATA "0000" ⊳ LEVEL 11

DATA "0010" ⊳ LEVEL 10

DATA "0011" ⊳ LEVEL 9

DATA "1011" ⊳ LEVEL 8

-------------------------------- DETERMINATION 7

DATA "1010" ⊳ LEVEL 7

DATA "1000" ⊳ LEVEL 6

DATA "1001" ⊳ LEVEL 5

DATA "1101" ⊳ LEVEL 4

DATA "1100" ⊳ LEVEL 3

DATA "1110" ⊳ LEVEL 2

DATA "1111" ⊳ LEVEL 1

BIT NUMBER

FIG.68

OR DATA OF
DL-1 AND DL-4
TO DL-4

DATA	I/O	DATA	I/O	DATA	I/O	DATA	I/O	DATA
	0	0	0	0	0	0	0	0
	1	0	1	0	1	0	1	0
	2	0	2	0	2	1	2	0
	3	0	3	0	3	1	3	0
	4	0	4	1	4	1	4	0
	5	0	5	1	5	1	5	0
	6	0	6	1	6	0	6	0
	7	0	7	1	7	0	7	0
	0	0	0	1	0	0	0	0
	1	1	1	1	1	0	1	1
	2	1	2	1	2	1	2	1
	3	0	3	1	3	1	3	0
	4	0	4	0	4	1	4	0
	5	0	5	0	5	1	5	1
	6	0	6	0	6	0	6	1
	7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4

OUTPUT
(0Fh-F0h)

OUTPUT
INVERTED
DATA
AFTER
OUTPUT
FROM DL-2
(3Ch-3Ch)

FIG.69

DATA "0111" ▷ LEVEL 16

DATA "0110" ▷ LEVEL 15

DATA "0100" ▷ LEVEL 14

DATA "0101" ▷ LEVEL 13

DATA "0001" ▷ LEVEL 12

DATA "0000" ▷ LEVEL 11

DATA "0010" ▷ LEVEL 10

THRESHOLD (V) DATA "0011" ▷ LEVEL 9

DATA "1011" ▷ LEVEL 8

DATA "1010" ▷ LEVEL 7

DATA "1000" ▷ LEVEL 6

- - - - - - - - - - - - - - - - - DETERMINATION 5

DATA "1001" ▷ LEVEL 5

DATA "1101" ▷ LEVEL 4

DATA "1100" ▷ LEVEL 3

DATA "1110" ▷ LEVEL 2

DATA "1111" ▷ LEVEL 1

BIT NUMBER

FIG.70

FIG.71

DATA "0111" ➤ LEVEL 16

DATA "0110" ➤ LEVEL 15

DATA "0100" ➤ LEVEL 14

DATA "0101" ➤ LEVEL 13

DATA "0001" ➤ LEVEL 12

DATA "0000" ➤ LEVEL 11

DATA "0010" ➤ LEVEL 10

------------------------------------ DETERMINATION 9

THRESHOLD (V) DATA "0011" ➤ LEVEL 9

DATA "1011" ➤ LEVEL 8

DATA "1010" ➤ LEVEL 7

DATA "1000" ➤ LEVEL 6

DATA "1001" ➤ LEVEL 5

DATA "1101" ➤ LEVEL 4

DATA "1100" ➤ LEVEL 3

DATA "1110" ➤ LEVEL 2

DATA "1111" ➤ LEVEL 1

BIT NUMBER

FIG.72

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0	0	0	0	0
0		1	0	1	0	1	0	1	0
0	NOR	2	0	2	0	2	1	2	0
0	INVERTED	3	0	3	0	3	1	3	0
0	DATA OF SL	4	0	4	1	4	1	4	0
1	AND DATA	5	1	5	1	5	1	5	0
1	OF DL-1	6	1	6	1	6	0	6	0
1	TO DL-1	7	0	7	1	7	0	7	0
1		0	0	0	1	0	0	0	0
1		1	0	1	1	1	0	1	1
1		2	0	2	1	2	1	2	1
1		3	0	3	1	3	1	3	0
1		4	0	4	0	4	1	4	0
1		5	0	5	0	5	1	5	1
1		6	0	6	0	6	0	6	1
1		7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	

OUTPUT (00h-FFh)

OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)

FIG.73

DATA "0111" ⊃ LEVEL 16

DATA "0110" ⊃ LEVEL 15

DATA "0100" ⊃ LEVEL 14

DATA "0101" ⊃ LEVEL 13

DATA "0001" ⊃ LEVEL 12
--- DETERMINATION 11

DATA "0000" ⊃ LEVEL 11

DATA "0010" ⊃ LEVEL 10

THRESHOLD (V) DATA "0011" ⊃ LEVEL 9

DATA "1011" ⊃ LEVEL 8

DATA "1010" ⊃ LEVEL 7

DATA "1000" ⊃ LEVEL 6

DATA "1001" ⊃ LEVEL 5

DATA "1101" ⊃ LEVEL 4

DATA "1100" ⊃ LEVEL 3

DATA "1110" ⊃ LEVEL 2

DATA "1111" ⊃ LEVEL 1

BIT NUMBER

FIG.74

OR DATA OF DL-1 AND DL-4
TO DL-4

DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
		0	0	0	0	0	0	0	0
		1	0	1	0	1	0	1	0
		2	0	2	0	2	1	2	0
		3	0	3	0	3	1	3	0
		4	0	4	1	4	1	4	0
		5	1	5	1	5	1	5	1
		6	1	6	1	6	0	6	1
		7	0	7	1	7	0	7	0
		0	0	0	1	0	0	0	0
		1	0	1	1	1	0	1	1
		2	0	2	1	2	1	2	1
		3	0	3	1	3	1	3	0
		4	0	4	0	4	1	4	0
		5	0	5	0	5	1	5	1
		6	0	6	0	6	0	6	1
		7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	

OUTPUT
(0Fh-F0h)

OUTPUT
INVERTED
DATA
AFTER
OUTPUT
FROM DL-2
(3Ch-3Ch)

FIG.75

DATA "0111" ⇒ LEVEL 16

DATA "0110" ⇒ LEVEL 15

DATA "0100" ⇒ LEVEL 14

DATA "0101" ⇒ LEVEL 13

DATA "0001" ⇒ LEVEL 12

---------------------------------- DETERMINATION 11

DATA "0000" ⇒ LEVEL 11

DATA "0010" ⇒ LEVEL 10

THRESHOLD (V) | DATA "0011" ⇒ LEVEL 9

DATA "1011" ⇒ LEVEL 8

DATA "1010" ⇒ LEVEL 7

DATA "1000" ⇒ LEVEL 6

DATA "1001" ⇒ LEVEL 5

DATA "1101" ⇒ LEVEL 4

DATA "1100" ⇒ LEVEL 3

DATA "1110" ⇒ LEVEL 2

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.76

DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
0		0	0	0	0	0	0	0	0
0		1	0	1	0	1	0	1	0
0	TO DL-1 →	2	0	2	0	2	1	2	0
1		3	1	3	0	3	1	3	0
1		4	1	4	1	4	1	4	0
1		5	1	5	1	5	1	5	1
1		6	1	6	1	6	0	6	1
1		7	1	7	1	7	0	7	0
1		0	1	0	1	0	0	0	0
1		1	1	1	1	1	0	1	1
1		2	1	2	1	2	1	2	1
1		3	1	3	1	3	1	3	0
1		4	1	4	0	4	1	4	0
1		5	1	5	0	5	1	5	1
1		6	1	6	0	6	0	6	1
1		7	1	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	

DL-2 OUTPUT (00h-FFh)

DL-3 OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)

FIG.77

DATA "0111" ⟩ LEVEL 16

DATA "0110" ⟩ LEVEL 15

DATA "0100" ⟩ LEVEL 14

----------------------------------- DETERMINATION 13

DATA "0101" ⟩ LEVEL 13

DATA "0001" ⟩ LEVEL 12

DATA "0000" ⟩ LEVEL 11

DATA "0010" ⟩ LEVEL 10

THRESHOLD (V) | DATA "0011" ⟩ LEVEL 9

DATA "1011" ⟩ LEVEL 8

DATA "1010" ⟩ LEVEL 7

DATA "1000" ⟩ LEVEL 6

DATA "1001" ⟩ LEVEL 5

DATA "1101" ⟩ LEVEL 4

DATA "1100" ⟩ LEVEL 3

DATA "1110" ⟩ LEVEL 2

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.78

OR DATA OF DL-1 AND DL-4
TO DL-4

DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
0		0	0	0	0	0	0	0	0
1		1	1	1	0	1	0	1	0
1		2	1	2	0	2	1	2	0
1		3	0	3	0	3	1	3	0
1		4	0	4	1	4	1	4	0
1		5	0	5	1	5	1	5	1
1		6	0	6	1	6	0	6	1
1		7	0	7	1	7	0	7	0
1		0	0	0	1	0	0	0	0
1		1	0	1	1	1	0	1	1
1		2	0	2	1	2	1	2	1
1		3	0	3	1	3	1	3	0
1		4	0	4	0	4	1	4	0
1		5	0	5	0	5	1	5	1
1		6	0	6	0	6	0	6	1
1		7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	

NOR INVERTED DATA OF SL AND DATA OF DL-1 TO DL-1

OUTPUT (0Fh-F0h)

OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)

FIG.79

DATA "0111" ➭ LEVEL 16

- DETERMINATION 15

DATA "0110" ➭ LEVEL 15

DATA "0100" ➭ LEVEL 14

DATA "0101" ➭ LEVEL 13

DATA "0001" ➭ LEVEL 12

DATA "0000" ➭ LEVEL 11

DATA "0010" ➭ LEVEL 10

THRESHOLD (V) DATA "0011" ➭ LEVEL 9

DATA "1011" ➭ LEVEL 8

DATA "1010" ➭ LEVEL 7

DATA "1000" ➭ LEVEL 6

DATA "1001" ➭ LEVEL 5

DATA "1101" ➭ LEVEL 4

DATA "1100" ➭ LEVEL 3

DATA "1110" ➭ LEVEL 2

DATA "1111" ➭ LEVEL 1

BIT NUMBER

FIG.80

OR DATA OF DL-1 AND DL-4
TO DL-4

DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
	0 [0]	0 [0]	0 [0]	0 [0]
	1 [1]	1 [0]	1 [0]	1 [1]
OR DATA	2 [1]	2 [0]	2 [1]	2 [1]
OF DL-1	3 [0]	3 [0]	3 [1]	3 [0]
AND DL-4	4 [0]	4 [1]	4 [1]	4 [0]
TO DL-4	5 [0]	5 [1]	5 [1]	5 [1]
	6 [0]	6 [1]	6 [0]	6 [1]
	7 [0]	7 [1]	7 [0]	7 [0]
	0 [0]	0 [1]	0 [0]	0 [0]
	1 [0]	1 [1]	1 [0]	1 [1]
	2 [0]	2 [1]	2 [1]	2 [1]
	3 [0]	3 [1]	3 [1]	3 [0]
	4 [0]	4 [0]	4 [1]	4 [0]
	5 [0]	5 [0]	5 [1]	5 [1]
	6 [0]	6 [0]	6 [0]	6 [1]
	7 [0]	7 [0]	7 [0]	7 [0]
SL	DL-1	DL-2	DL-3	DL-4

OUTPUT
(0Fh-F0h)

OUTPUT
INVERTED
DATA
AFTER
OUTPUT
FROM DL-2
(3Ch-3Ch)

FIG.81

THRESHOLD (V)

DATA "0111" ⟹ LEVEL 16

------------------------- DETERMINATION 15

DATA "0110" ⟹ LEVEL 15

DATA "0100" ⟹ LEVEL 14

DATA "0101" ⟹ LEVEL 13

DATA "0001" ⟹ LEVEL 12

DATA "0000" ⟹ LEVEL 11

DATA "0010" ⟹ LEVEL 10

DATA "0011" ⟹ LEVEL 9

DATA "1011" ⟹ LEVEL 8

DATA "1010" ⟹ LEVEL 7

DATA "1000" ⟹ LEVEL 6

DATA "1001" ⟹ LEVEL 5

DATA "1101" ⟹ LEVEL 4

DATA "1100" ⟹ LEVEL 3

DATA "1110" ⟹ LEVEL 2

DATA "1111" ⟹ LEVEL 1

BIT NUMBER

FIG.82

FIG.83

FIG.84

I/O DATA		I/O DATA		I/O DATA	I/O DATA	DATA		
0	0	0	1	0	0		1	0
1	0	1	1	1	1		1	0
2	0	2	1	2	2		1	0
3	0	3	1	3	3		1	0
4	0	4	0	4	4	FROM	1	1
5	0	5	0	5	5	OPERATION	1	1
6	0	6	0	6	6	OF DATA	1	1
7	0	7	0	7	7	OF DL-1	1	1
0	1	0	0	0	0	AND DL-2	0	1
1	1	1	0	1	1		0	1
2	1	2	0	2	2		0	1
3	1	3	0	3	3		0	1
4	1	4	1	4	4		1	1
5	1	5	1	5	5		1	1
6	1	6	1	6	6		1	1
7	1	7	1	7	7		1	1
DL-1		DL-2		DL-3	DL-4		SL	SL

WHEN AT LEVEL 5   WHEN AT LEVEL 13

FIG.85

DATA "0101" ⇒ LEVEL 13
— — — — — — — — — — — DETERMINATION 12

THRESHOLD (V) DATA "0011" ⇒ LEVEL 9
— — — — — — — — — — — DETERMINATION 8

DATA "1001" ⇒ LEVEL 5
— — — — — — — — — — — DETERMINATION 4

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.86

FIG.87

DATA "0110" ⟩ LEVEL 15

- DETERMINATION 14

DATA "0101" ⟩ LEVEL 13

DATA "0000" ⟩ LEVEL 11

- DETERMINATION 10

THRESHOLD (V) | DATA "0011" ⟩ LEVEL 9

DATA "1010" ⟩ LEVEL 7

- DETERMINATION 6

DATA "1001" ⟩ LEVEL 5

DATA "1100" ⟩ LEVEL 3

- DETERMINATION 2

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.88

	I/O DATA	I/O DATA	I/O DATA			DATA
0		0 [1]	0		0	[0]
1		1 [1]	1		1	[0]
2		2 [1]	2		2	[0]
3		3 [1]	3	FROM DL-1	3	[0]
4		4 [0]	4		4	[0]
5		5 [0]	5		5	[0]
6		6 [0]	6		6	[0]
7		7 [0]	7		7	[0]
0		0 [0]	0		0	[1]
1		1 [0]	1		1	[1]
2		2 [0]	2		2	[1]
3		3 [0]	3		3	[1]
4		4 [1]	4		4	[1]
5		5 [1]	5		5	[1]
6		6 [1]	6		6	[1]
7		7 [1]	7		7	[1]

DL-1   DL-2   DL-3   SL

INPUT

FIG.89

THRESHOLD (V) DATA "0011" ⟩ LEVEL 9
- DETERMINATION 8

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.90

I/O DATA	I/O DATA	I/O DATA		DATA	
0 ☐	0 [1]	0 [1]		[1]	0
1 ☐	1 [1]	1 [1]	OPERATE DATA	[1]	0
2 ☐	2 [1]	2 [0]	OF SL AND DL-2	[1]	0
3 ☐	3 [1]	3 [0]		[1]	0
4 ☐	4 [0]	4 [0]		[1]	1
5 ☐	5 [0]	5 [0]		[1]	1
6 ☐	6 [0]	6 [1]		[1]	1
7 ☐	7 [0]	7 [1]		[1]	1
0 ☐	0 [0]	0 [1]		[0]	1
1 ☐	1 [0]	1 [1]		[0]	1
2 ☐	2 [0]	2 [0]		[0]	1
3 ☐	3 [0]	3 [0]		[0]	1
4 ☐	4 [1]	4 [0]		[1]	1
5 ☐	5 [1]	5 [0]		[1]	1
6 ☐	6 [1]	6 [1]		[1]	1
7 ☐	7 [1]	7 [1]		[1]	1
DL-1	DL-2	DL-3		SL	LEVEL 13
		INPUT		LEVEL 5	

FIG.91

DATA "0101" ⟩ LEVEL 13

------------------------------- DETERMINATION 12

THRESHOLD (V)   DATA "0011" ⟩ LEVEL 9

DATA "1001" ⟩ LEVEL 5

------------------------------- DETERMINATION 4

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.92

	I/O DATA		I/O DATA		I/O DATA		DATA
0	1	0	1	0	1		0
1	1	1	0	1	1		0
2	1	2	0	2	0		0
3	1	3	1	3	0		0
4	1	4	1	4	0		0
5	1	5	0	5	0		0
6	1	6	0	6	1		0
7	1	7	1	7	1		0
0	0	0	1	0	1		1
1	0	1	0	1	1		1
2	0	2	0	2	0		1
3	0	3	1	3	0		1
4	0	4	1	4	0		1
5	0	5	0	5	0		1
6	0	6	0	6	1		1
7	0	7	1	7	1		1
	DL-1		DL-2		DL-3		SL

INVERTED DATA OF SL TO DL-1

INPUT

READ AT DETERMINATION 8

FIG.93

FIG.94

I/O DATA	I/O DATA	I/O DATA		DATA
0 [1]	0 [1]	0 [1]		[0]
1 [1]	1 [0]	1 [1]		[0]
2 [1]	2 [0]	2 [0]	OR DATA OF SL	[0]
3 [1]	3 [1]	3 [0]	AND DL-1 AND	[0]
4 [1]	4 [1]	4 [0]	STORE RESULT	[0]
5 [1]	5 [0]	5 [0]	IN DL-1	[0]
6 [1]	6 [0]	6 [1]		[0]
7 [1]	7 [1]	7 [1]		[0]
0 [0]	0 [1]	0 [1]		[0]
1 [0]	1 [0]	1 [1]		[0]
2 [0]	2 [0]	2 [0]		[0]
3 [0]	3 [1]	3 [0]		[0]
4 [1]	4 [1]	4 [0]		[1]
5 [1]	5 [0]	5 [0]		[1]
6 [1]	6 [0]	6 [1]		[1]
7 [1]	7 [1]	7 [1]		[1]
DL-1	DL-2	DL-3		SL
	INPUT			READ AT DETERMINATION 4

FIG.95

DATA "0101" ⟩ LEVEL 13

THRESHOLD (V)   DATA "0011" ⟩ LEVEL 9

DATA "1001" ⟩ LEVEL 5
- DETERMINATION 4

DATA "1111" ⟩ LEVEL 1
BIT NUMBER

FIG.96

I/O DATA	I/O DATA	I/O DATA		DATA
0 [1]	0 [1]	0 [1]		[1]
1 [1]	1 [0]	1 [1]		[1]
2 [1]	2 [0]	2 [0]	OPERATE DATA	[1]
3 [1]	3 [1]	3 [0]	OF SL AND DL-3	[1]
4 [1]	4 [1]	4 [0]		[1]
5 [1]	5 [0]	5 [0]		[1]
6 [1]	6 [0]	6 [1]		[1]
7 [1]	7 [1]	7 [1]		[1]
0 [0]	0 [1]	0 [1]		[1]
1 [0]	1 [0]	1 [1]		[1]
2 [0]	2 [0]	2 [0]		[1]
3 [0]	3 [1]	3 [0]		[1]
4 [1]	4 [1]	4 [0]		[0]
5 [1]	5 [0]	5 [0]		[0]
6 [1]	6 [0]	6 [1]		[1]
7 [1]	7 [1]	7 [1]		[1]
DL-1	DL-2	DL-3		SL
	INPUT			WRITE LEVEL 3

FIG.97

THRESHOLD (V)

DATA "0101" ⟩ LEVEL 13

DATA "0011" ⟩ LEVEL 9

DATA "1001" ⟩ LEVEL 5

DATA "1100" ⟩ LEVEL 3
- DETERMINATION 2

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.98

I/O	DATA	I/O	DATA	I/O	DATA		DATA
0	1	0	1	0	1		1
1	1	1	0	1	1		1
2	1	2	0	2	0		1
3	1	3	1	3	0		1
4	1	4	1	4	0		1
5	1	5	0	5	0		1
6	1	6	0	6	1		1
7	1	7	1	7	1		-1
0	0	0	1	0	1		0
1	0	1	0	1	1		0
2	0	2	0	2	0		1
3	0	3	1	3	0		1
4	1	4	1	4	0		1
5	1	5	0	5	0		1
6	1	6	0	6	1		1
7	1	7	1	7	1		1
DL-1		DL-2		DL-3			SL
		INPUT					WRITE LEVEL 7

OPERATE DATA OF DL-1 AND DL-3 TO SL

FIG.99

DATA "0101" ⟹ LEVEL 13

THRESHOLD (V) DATA "0011" ⟹ LEVEL 9

DATA "1001" ⟹ LEVEL 7

- DETERMINATION 6

DATA "1001" ⟹ LEVEL 5

DATA "1100" ⟹ LEVEL 3

DATA "1111" ⟹ LEVEL 1

BIT NUMBER

FIG.100

I/O	DATA	I/O	DATA	I/O	DATA			DATA
0	0	0	1	0	1			0
1	0	1	0	1	1			0
2	0	2	0	2	0	←→		0
3	0	3	1	3	0	TRANSFER		0
4	0	4	1	4	0	FROM SL		0
5	0	5	0	5	0	TO DL-1		0
6	0	6	0	6	1			0
7	0	7	1	7	1			0
0	1	0	1	0	1			1
1	1	1	0	1	1			1
2	1	2	0	2	0			1
3	1	3	1	3	0			1
4	1	4	1	4	0			1
5	1	5	0	5	0			1
6	1	6	0	6	1			1
7	1	7	1	7	1			1
	DL-1		DL-2		DL-3			SL
			INPUT					READ AT
								DETERMINATION 8

FIG.101

THRESHOLD (V)

DATA "0101" ▷ LEVEL 13

DATA "0011" ▷ LEVEL 9
- DETERMINATION 8

DATA "1001" ▷ LEVEL 7

DATA "1001" ▷ LEVEL 5

DATA "1100" ▷ LEVEL 3

DATA "1111" ▷ LEVEL 1

BIT NUMBER

FIG.102

I/O DATA		I/O DATA		I/O DATA			DATA	
0	1	0	1	0	1		0	
1	1	1	0	1	1		0	
2	1	2	0	2	0	OR INVERTED	0	
3	1	3	1	3	0	DATA OF SL	0	
4	0	4	1	4	0	AND DATA OF	1	
5	0	5	0	5	0	DL-1 AND	1	
6	0	6	0	6	1	STORE RESULT	1	
7	0	7	1	7	1	IN DL-1	1	
0	1	0	1	0	1		1	
1	1	1	0	1	1		1	
2	1	2	0	2	0		1	
3	1	3	1	3	0		1	
4	1	4	1	4	0		1	
5	1	5	0	5	0		1	
6	1	6	0	6	1		1	
7	1	7	1	7	1		1	

DL-1   DL-2   DL-3   SL

INPUT

READ AT
DETERMINATION 12

FIG.103

DATA "0101" ⇒ LEVEL 13

-- DETERMINATION 12

THRESHOLD (V) DATA "0011" ⇒ LEVEL 9

DATA "1010" ⇒ LEVEL 7

DATA "1001" ⇒ LEVEL 5

DATA "1100" ⇒ LEVEL 3

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.104

FIG.105

THRESHOLD (V)

DATA "0101" ⟩ LEVEL 13

DATA "0000" ⟩ LEVEL 11
------------------------------ DETERMINATION 10

DATA "0011" ⟩ LEVEL 9

DATA "1010" ⟩ LEVEL 7

DATA "1001" ⟩ LEVEL 5

DATA "1100" ⟩ LEVEL 3

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.106

I/O DATA		I/O DATA		I/O DATA		DATA
0	1	0	1	0	1	0
1	1	1	0	1	1	0
2	1	2	0	2	0	0
3	1	3	1	3	0	0
4	0	4	1	4	0	1
5	0	5	0	5	0	1
6	0	6	0	6	1	1
7	0	7	1	7	1	1
0	0	0	1	0	1	1
1	0	1	0	1	1	1
2	0	2	0	2	0	1
3	0	3	1	3	0	1
4	1	4	1	4	0	1
5	1	5	0	5	0	1
6	1	6	0	6	1	1
7	1	7	1	7	1	1
DL-1		DL-2		DL-3		SL

OPERATE DATA OF DL-1 AND DL-3 TO SL

INPUT

READ AT DETERMINATION 12

FIG.107

THRESHOLD (V)

DATA "0101" ⟩ LEVEL 13

-- DETERMINATION 12

DATA "0000" ⟩ LEVEL 11

DATA "0011" ⟩ LEVEL 9

DATA "1010" ⟩ LEVEL 7

DATA "1001" ⟩ LEVEL 5

DATA "1100" ⟩ LEVEL 3

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.108

I/O DATA		I/O DATA		I/O DATA			DATA	
0		0	1	0	1		0	
1		1	0	1	1		0	
2		2	0	2	0		1	
3		3	1	3	0		1	
4		4	1	4	0		1	
5		5	0	5	0		1	
6		6	0	6	1		1	
7		7	1	7	1		1	
0		0	1	0	1		1	
1		1	0	1	1		1	
2		2	0	2	0		1	
3		3	1	3	0		1	
4		4	1	4	0		1	
5		5	0	5	0		1	
6		6	0	6	1		1	
7		7	1	7	1		1	

DL-1	DL-2	DL-3	SL
	INPUT		WRITE LEVEL 15

FIG.109

THRESHOLD (V)

DATA "0110" ⟹ LEVEL 15
------------------------------ DETERMINATION 14

DATA "0101" ⟹ LEVEL 13

DATA "0000" ⟹ LEVEL 11

DATA "0011" ⟹ LEVEL 9

DATA "1010" ⟹ LEVEL 7

DATA "1001" ⟹ LEVEL 5

DATA "1100" ⟹ LEVEL 3

DATA "1111" ⟹ LEVEL 1

BIT NUMBER

FIG.110

I/O	DATA	I/O	DATA	I/O	DATA
0	0	0	1	0	
1	0	1	0	1	
2	0	2	0	2	
3	0	3	1	3	
4	0	4	1	4	
5	0	5	0	5	
6	0	6	0	6	
7	0	7	1	7	
0	0	0	1	0	
1	0	1	0	1	
2	0	2	0	2	
3	0	3	1	3	
4	0	4	1	4	
5	0	5	0	5	
6	1	6	0	6	
7	1	7	1	7	

DL-1   DL-2   DL-3

TRANSFER FROM SL TO DL-1 OPERATE DATA OF SL AND DL-2 TO SL

DATA
0
0
0
0
0
0
0
0
0
0
0
0
0
0
1
1

SL

READ AT DETERMINATION 2

FIG.111

DATA "0110" ⇒ LEVEL 15

DATA "0101" ⇒ LEVEL 13

DATA "0000" ⇒ LEVEL 11

THRESHOLD (V) DATA "0011" ⇒ LEVEL 9

DATA "1010" ⇒ LEVEL 7

DATA "1001" ⇒ LEVEL 5

DATA "1100" ⇒ LEVEL 3

-- DETERMINATION 2

DATA "1111" ⇒ LEVEL 1

BIT NUMBER

FIG.112

I/O	DATA	I/O	DATA	I/O	DATA		DATA
0	0	0	1	0			1
1	0	1	0	1			1
2	0	2	0	2			1
3	0	3	1	3			1
4	0	4	1	4			1
5	0	5	0	5			1
6	0	6	0	6			1
7	0	7	1	7			1
0	0	0	1	0			1
1	0	1	0	1			1
2	0	2	0	2			1
3	0	3	1	3			1
4	0	4	1	4			1
5	0	5	0	5			1
6	1	6	0	6			0
7	1	7	1	7			1
	DL-1		DL-2		DL-3		SL

WRITE LEVEL 2

FIG.113

DATA "0110" ⟩ LEVEL 15

DATA "0101" ⟩ LEVEL 13

DATA "0000" ⟩ LEVEL 11

THRESHOLD (V) | DATA "0011" ⟩ LEVEL 9

DATA "1010" ⟩ LEVEL 7

DATA "1001" ⟩ LEVEL 5

DATA "1100" ⟩ LEVEL 3

DATA "1110" ⟩ LEVEL 2

--- DETERMINATION 1

DATA "1111" ⟩ LEVEL 1

BIT NUMBER

FIG.114

I/O DATA	DL-1	I/O DATA	DL-2	I/O DATA	DL-3	DATA SL
0	1	0	1	0		0
1	1	1	0	1		0
2	1	2	0	2		0
3	1	3	1	3		0
4	1	4	1	4		0
5	1	5	0	5		0
6	1	6	0	6		0
7	1	7	1	7		0
0	1	0	1	0		0
1	1	1	0	1		0
2	1	2	0	2		0
3	1	3	1	3		0
4	0	4	1	4		1
5	0	5	0	5		1
6	1	6	0	6		1
7	1	7	1	7		1

OR INVERTED DATA OF SL AND DATA OF DL-1 AND STORE RESULT IN DL-1

READ AT DETERMINATION 4

FIG.115

FIG.116

I/O DATA		I/O DATA		I/O DATA			DATA	
0	1	0	1	0			1	
1	1	1	0	1			1	
2	1	2	0	2		OPERATE DATA	1	
3	1	3	1	3		OF DL-1 AND	1	
4	1	4	1	4		DL-2	1	
5	1	5	0	5		TO SL	1	
6	1	6	0	6			1	
7	1	7	1	7			1	
0	1	0	1	0			1	
1	1	1	0	1			1	
2	1	2	0	2			1	
3	1	3	1	3			1	
4	0	4	1	4			0	
5	0	5	0	5			1	
6	1	6	0	6			1	
7	1	7	1	7			1	
DL-1		DL-2		DL-3			SL	

WRITE LEVEL 4

FIG.117

DATA "0110" LEVEL 15

DATA "0101" LEVEL 13

DATA "0000" LEVEL 11

THRESHOLD (V) DATA "0011" LEVEL 9

DATA "1010" LEVEL 7

DATA "1001" LEVEL 5

DATA "1001" LEVEL 4

- DETERMINATION 3

DATA "1100" LEVEL 3

DATA "1110" LEVEL 2

DATA "1111" LEVEL 1

BIT NUMBER

FIG.118
PRIOR ART

8000

ADDRESS BUFFER/DATA INPUT/OUTPUT BUFFER — 140

DQ0 ··· DQj A0 ··· Ak
10   12

CHIP CONTROL PART — 200

POWER SUPPLY GENERATION PART — 150

ROW DECODER — 110

MEMORY ARRAY PART

COLUMN DECODER — 130

DATA LATCH (DL-R) — 20

ROW DECODER — 110

SENSE LATCH (SL) — 120

COLUMN DECODER — 130

ROW DECODER — 100R

18

WL BL

MEMORY ARRAY PART

ROW DECODER — 110

COLUMN DECODER — 130

COLUMN DECODER — 130

ROW DECODER — 100L

DATA LATCH L (DL-L) — 20

FIG.119 PRIOR ART

THRESHOLD (V)

DATA "0"   LEVEL 2

----- DETERMINATION LEVEL Vj01

DATA "1"   LEVEL 1

BIT NUMBER

FIG.120 PRIOR ART

THRESHOLD (V)

DATA "01"   LEVEL 4

----- DETERMINATION LEVEL Vj3

DATA "00"   LEVEL 3

----- DETERMINATION LEVEL Vj2

DATA "10"   LEVEL 2

----- DETERMINATION LEVEL Vj1

DATA "11"   LEVEL 1

BIT NUMBER

FIG. 121 PRIOR ART

```
   I/O DATA    I/O DATA              DATA
DQ4 [ 0 ]   DQ0 [ 1 ]            [ 0 ] ⟶ MC4
DQ5 [ 0 ]   DQ1 [ 0 ]            [ 1 ] ⟶ MC3
DQ6 [ 1 ]   DQ2 [ 0 ]  OPERATION [ 1 ] ⟶ MC2
DQ7 [ 1 ]   DQ3 [ 1 ]            [ 1 ] ⟶ MC1
    DL-L        DL-R                 SL
       INPUT (C9h)
```

FIG. 122 PRIOR ART

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

- - - - - - - - - - - - - - - - DETERMINATION 3

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.123 PRIOR ART

	I/O DATA		I/O DATA			DATA	
4	0	0	1			1	
5	0	1	0			0	
6	1	2	0	OPERATION	→	1	
7	1	3	1			1	
	DL-L		DL-R			SL	

FIG.124 PRIOR ART

THRESHOLD (V)

DATA "00" ──▷ LEVEL 3 ------ DETERMINATION 3
------ DETERMINATION 2

DATA "11" ──▷ LEVEL 1

BIT NUMBER

FIG.125 PRIOR ART

```
 I/O DATA   I/O DATA              DATA
  4 │ 0 │    0 │ 1 │               │ 1 │
  5 │ 0 │    1 │ 0 │               │ 1 │
  6 │ 1 │    2 │ 0 │  OPERATION    │ 0 │
  7 │ 1 │    3 │ 1 │  ────────→    │ 1 │
    DL-L        DL-R                 SL
```

FIG.126 PRIOR ART

THRESHOLD (V) ┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄ DETERMINATION 2

DATA "10" LEVEL 2

┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄┄ DETERMINATION 1

DATA "11" LEVEL 1

BIT NUMBER

FIG.127 PRIOR ART

DATA

SL
0
0
0
1

→

I/O DATA

	DL-L
4	
5	
6	
7	

I/O DATA

	DL-R
0	0
1	0
2	0
3	1

FIG.128 PRIOR ART

THRESHOLD (V)

DATA "01" ⟩ LEVEL 4

DATA "00" ⟩ LEVEL 3

DATA "10" ⟩ LEVEL 2

----------- DETERMINATION 1

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.129 PRIOR ART

DATA

0	
0	
1	
1	

SL

I/O DATA

4	0
5	0
6	1
7	1

DL-L

I/O DATA

0	0
1	0
2	0
3	1

DL-R

FIG.130 PRIOR ART

DATA "01" ⟩ LEVEL 4

DATA "00" ⟩ LEVEL 3

THRESHOLD (V) ---------------------------------- DETERMINATION 2

DATA "10" ⟩ LEVEL 2

DATA "11" ⟩ LEVEL 1

BIT NUMBER

FIG.131 PRIOR ART

DATA

| 0 |
| 1 |
| 1 |
| 1 |

SL

→ OPERATION →

I/O DATA

4	0
5	0
6	1
7	1

DL-L

I/O DATA

0	1
1	0
2	0
3	1

DL-R

OUTPUT (C9h)

FIG.132 PRIOR ART

THRESHOLD (V)

DATA "01" → LEVEL 4

------------------------------------- DETERMINATION 3

DATA "00" → LEVEL 3

DATA "10" → LEVEL 2

DATA "11" → LEVEL 1

BIT NUMBER